WHAT IS CLAIMED IS

1. A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the Young's modulus of a first dielectric layer in which the via holes are formed is relatively smaller than the Young's modulus of a second dielectric layer in which wiring grooves are formed.

2. A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the Young's modulus of a first dielectric layer in which the via holes are formed is relatively smaller than the Young's modulus of a second dielectric layer in which the wiring grooves are formed, and the specific dielectric constant of the first dielectric layer is relatively smaller than the specific dielectric constant of the second dielectric layer.

3. A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the

wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the Young's modulus of a first dielectric layer in which the via holes are formed is relatively smaller than the Young's modulus of a second dielectric layer in which the wiring grooves are formed, and the hole diameter of the via hole is about 0.5 μm or less.

4. A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the Young's modulus of a first dielectric layer in which the via holes are formed is relatively smaller than the Young's modulus of a second dielectric layer in which the wiring grooves are formed, and a stopper dielectric film of a relatively thin film thickness is formed between the first dielectric layer and the second dielectric layer.

5. A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the Young's modulus of a first dielectric layer in which the via holes are formed is relatively smaller

than the Young's modulus of a second dielectric layer in which the wiring grooves are formed, and a main conductive layer constituting the wirings is made of copper.

6. A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the Young's modulus of the first dielectric layer in which the via holes are formed is less than 60 GPa and the Young's modulus of the second dielectric layer in which the wiring grooves are formed is 60 GPa or more.

7. A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the first dielectric layer in which the via holes are formed is constituted of SiOF and the second dielectric layer in which the wiring grooves are formed is constituted of SiO_2.

8. A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower

layer wirings thereof,

wherein the first dielectric layer in which the via holes are formed is constituted of SiOF and the second dielectric layer in which the wiring grooves are formed is constituted of SiO_2, and the hole diameter of the via hole is about 0.5 μm or less.

9. A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the first dielectric layer in which the via holes are formed is constituted of SiOF and the second dielectric layer in which the wiring grooves are formed is constituted of SiO_2, and a stopper dielectric film of relatively thin film thickness comprising SiN or SiC is formed between the first dielectric layer and the second dielectric layer.

10. A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the Young's modulus of the first dielectric layer in which the via holes are formed is less than 30 GPa,

and the Young's modulus of the second dielectric layer in which the wiring grooves are formed is 30 GPa or more.

11. A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the first dielectric layer in which the via holes are formed is constituted of an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, and the second dielectric layer in which the wiring grooves are formed is constituted of SiOF or SiO_2.

12. A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the first dielectric layer in which the via holes are formed is constituted of an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, and the second dielectric layer in which the wiring grooves are formed is constituted of SiOF or SiO_2, and the hole diameter of the via hole is about 0.2 μm or less.

13. A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the first dielectric layer in which the via holes are formed is constituted of an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, and the second dielectric layer in which the wiring grooves are formed is constituted of SiOF or SiO_2, and a stopper dielectric film of relatively thin film thickness comprising SiN or SiC is formed between the first dielectric layer and the second dielectric layer.

14. A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the Young's modulus of the first dielectric layer in which the via holes are formed is less than 6 GPa and the Young's modulus of the second dielectric layer in which the wiring grooves are formed is 6 GPa or more.

15. A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the

wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the first dielectric layer in which the via holes are formed is constituted of a porous HSQ type material and the second dielectric layer in which the wiring grooves are formed is constituted of an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, or a laminate of an SiO_2 with an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material.

16. A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the first dielectric layer in which the via holes are formed is constituted of a porous HSQ type material and the second dielectric layer in which the wiring grooves are formed is constituted of an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, or a laminate of an SiO_2 with an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, and the hole diameter of the via hole is about 0.13 μm or less.

17. A semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof,

wherein the first dielectric layer in which the via holes are formed is constituted of a porous HSQ type material and the second dielectric layer in which the wiring grooves are formed is constituted of an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, or a laminate of an SiO_2 with an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, and a stopper dielectric film of a relatively thin film thickness comprising SiO_2 is formed between the first dielectric layer and the second dielectric layer.

18. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer having a relatively small Young's modulus and a second dielectric layer having a relatively large Young's modulus successively on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves.

19. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer having a relatively small Young's modulus and a second dielectric layer having a relatively large Young's modulus successively on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves,

wherein the specific dielectric constant of the first dielectric layer is less than the specific dielectric constant of the second dielectric layer.

20. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member

formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer having a relatively small Young's modulus and a second dielectric layer having a relatively large Young's modulus successively on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves,

wherein the hole diameter of the via hole is about 0.5 μm or less.

21. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer having a relatively small Young's modulus and a second dielectric layer having a relatively large Young's modulus successively on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves,

wherein a stopper dielectric film of a relatively thin film thickness is formed to an upper layer of the first dielectric layer in the step (a) and wiring grooves are formed at a predetermined region in the second dielectric layer and the stopper dielectric film.

22. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer having a relatively small Young's modulus and a second dielectric layer having a relatively large Young's modulus successively on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves,

wherein a main conductive layer buried inside the via holes and the wiring grooves in the step (c) comprises copper.

23. A method of fabricating a semiconductor device having

wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer having a Young's modulus of less than 60 GPa and a second dielectric layer having a Young's modulus of 60 GPa or more on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves.

24. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer having a Young's modulus of less than 60 GPa and a second dielectric layer having a Young's modulus of 60 GPa or more on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the

wiring grooves,

wherein the first dielectric layer and the second dielectric layer are formed by a CVD method.

25. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer constituted of SiOF and a second dielectric layer constituted of SiO_2 on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves.

26. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer constituted of SiOF and a second dielectric layer constituted of SiO_2 on a substrate,

(b) forming the via holes at predetermined regions of the

first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves,

wherein the hole diameter of the via hole is about 0.5 μm or less.

27. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer constituted of SiOF and a second dielectric layer constituted of SiO_2 on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves,

wherein a stopper dielectric film comprising SiN or SiC of a relatively thin thickness is formed to an upper layer of the first dielectric layer in the step (a) and wiring grooves are formed at predetermined regions in the second dielectric layer and the stopper dielectric film.

28. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer having a Young's modulus of less than 30 GPa and a second dielectric layer having a Young's modulus of 30 GPa or more on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves.

29. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer having a Young's modulus of less than 30 GPa and a second dielectric layer having a Young's modulus of 30 GPa or more on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves,

wherein the first dielectric layer is formed by a CVD method or coating method and the second dielectric layer are formed by a CVD method

30. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer constituted of an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material and a second dielectric layer is constituted of SiOF or SiO_2 successively on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves.

31. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for

connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer constituted of an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material and a second dielectric layer is constituted of SiOF or SiO_2 successively on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves,

wherein the hole diameter of the via hole is about 0.2 μm or less.

32. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer constituted of an SiOC type material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material and a second dielectric layer is constituted of SiOF or SiO_2 successively on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves,

wherein a stopper dielectric film comprising SiN or SiC of a relatively thin film thickness is formed to an upper layer of the first dielectric layer in the step (a) and wiring grooves are formed at a predetermined region in the second dielectric layer and the stopper dielectric film in the step (b).

33. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer having a Young's modulus of less than 6 GPa and a second dielectric layer having a Young's modulus of 6 GPa or more on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves.

34. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer having a Young's modulus of less than 6 GPa and a second dielectric layer having a Young's modulus of 6 GPa or more on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves,

wherein the first dielectric layer is formed by a coating method and the second dielectric layer are formed by a CVD method or coating method.

35. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer constituted of a porous HSQ type material and a second dielectric layer constituted

of an SiOC material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, or a laminate of SiO_2 with an SiOC type material, CF type material, HSQ type material, MSQ type material BCB type material or PAE type material successively on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves.

36. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer constituted of a porous HSQ type material and a second dielectric layer constituted of an SiOC material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, or a laminate of SiO_2 with an SiOC type material, CF type material, HSQ type material, MSQ type material BCB type material or PAE type material successively on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at

predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves,

wherein the hole diameter of the via hole is about 0.13 μm or less.

37. A method of fabricating a semiconductor device having wirings formed in wiring grooves and a connection member formed integrally with the wirings in via holes for connecting the wirings and lower layer wirings thereof comprising the steps of:

(a) forming a first dielectric layer constituted of a porous HSQ type material and a second dielectric layer constituted of an SiOC material, CF type material, HSQ type material, MSQ type material, BCB type material or PAE type material, or a laminate of SiO_2 with an SiOC type material, CF type material, HSQ type material, MSQ type material BCB type material or PAE type material successively on a substrate,

(b) forming the via holes at predetermined regions of the first dielectric layer and forming the wiring grooves at predetermined regions of the second dielectric layer, and

(c) burying a conductive member inside the via holes and the wiring grooves,

wherein a stopper dielectric film comprising SiO_2 of relatively thin film thickness is formed to an upper layer of

the first dielectric layer in the step (a) and wiring grooves are formed at predetermined regions in the second dielectric layer and the stopper dielectric film in the step (b).